CLAIMS

1. A negative voltage generator for a semiconductor memory device comprising:

a first charge pump having an output; and

a second charge pump having an output coupled to the output of the first charge pump, wherein the second charge pump is adapted to be controlled by a precharge signal.

2. A negative voltage generator according to claim 1 further comprising a negative voltage regulator having an input coupled to the output of the first charge pump and an output coupled to the output of the second charge pump.

3. A negative voltage generator according to claim 1 wherein the output of the first charge pump is connected directly to the output of the second charge pump.

4. A negative voltage generator according to claim 3 further comprising a negative voltage regulator having an input coupled to the outputs of the first and second charge pumps.

5. A negative voltage generator according to claim 1 further comprising a level detector having an input coupled to the output of the first negative charge pump.

6. A negative voltage generator according to claim 1 wherein the precharge signal is a word-line precharge signal.

7. A negative voltage generator for a semiconductor memory device comprising:

first means for pumping charge to a negative voltage source; and

second means for pumping charge to the negative voltage source, wherein the second means for pumping charge is adapted to be controlled by a precharge signal.

8. A negative voltage generator according to claim 7 wherein the first means for pumping charge has an output connected directly to an output of the second means for pumping charge.

9. A negative voltage generator according to claim 7 further comprising means for regulating the negative voltage source.

10. A negative voltage generator according to claim 9 wherein:

the first means for pumping charge has an output connected directly to an output of the second means for pumping charge; and

the means for regulating the negative voltage source has in input coupled to an output of the first means for pumping charge and an output of the second means for pumping charge.

11. A negative voltage generator according to claim 9 wherein the means for regulating the negative voltage source has in input coupled to an output of the first means for pumping charge and an output coupled to an output of the second means for pumping charge.

12. A negative voltage generator according to claim 7 further comprising means for detecting the voltage level of the negative voltage source.

13. A negative voltage generator according to claim 7 wherein the negative voltage source is a negative voltage source for negatively biasing a word line.

14. A negative voltage generator for a semiconductor memory device comprising:

an oscillator;

a first charge pump having an input coupled to the oscillator and an output for generating a first negative voltage responsive to an oscillating signal from the oscillator;

a negative voltage regulator having an input coupled to the output of the negative voltage generator and an output for generating a second negative voltage responsive to the first negative voltage; and

a second charge pump having an output coupled to the output of the negative voltage regulator, wherein the second charge pump is adapted to be controlled by a word-line precharge signal.

15. A negative voltage generator according to claim 14 further comprising a level detector having an input coupled to the output of the first charge pump and an output coupled to the oscillator.

16. A negative voltage generator according to claim 14 wherein the second charge pump is adapted to pump a predetermined amount of charge to the second negative voltage responsive to the word-line precharge signal.

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17. A method for operating a semiconductor memory device comprising controlling a negative voltage generator responsive to a precharge signal.

18. A method according to claim 17 wherein:

the negative voltage generator comprises a first charge pump and a second charge pump; and

controlling a negative voltage generator responsive to a precharge signal comprises activating the second charge pump responsive to the precharge signal.

19. A method according to claim 18 wherein the first charge pump generates a first negative voltage.

20. A method according to claim 19 wherein activating the second charge pump responsive to the precharge signal comprises coupling charge from the second charge pump to the first negative voltage.

21. A method according to claim 19 further comprising regulating the first negative voltage, thereby generating a second negative voltage.

22. A method according to claim 21 wherein activating the second charge pump responsive to the precharge signal comprises coupling charge from the second charge pump to the second negative voltage.

23. A method according to claim 18 wherein activating the second charge pump responsive to the precharge signal comprises supplying a predetermined amount of charge from the second charge pump.

24. A method according to claim 17 wherein the precharge signal is a word-line precharge signal.

25. A negative voltage level detector for a semiconductor device comprising:

a differential amplifier having a first input and a second input;

a first voltage divider coupled to the first input of the differential amplifier; and

a second voltage divider coupled to the second input of the differential amplifier, and adapted to drive the second input of the differential amplifier responsive to a negative voltage.

26. A negative voltage level detector according to claim 25 wherein the first voltage divider is adapted to drive the first input of the differential amplifier responsive to a reference voltage.

27. A negative voltage level detector according to claim 26 wherein the first voltage divider comprises:

a first resistor coupled between the reference voltage and the first input of the differential amplifier; and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal.

28. A negative voltage level detector according to claim 26 wherein the second voltage divider comprises:

a first resistor coupled between a reference voltage and the second input of the differential amplifier; and

a second resistor coupled between the second input of the differential amplifier and the negative voltage.

29. A negative voltage level detector according to claim 25 further comprising an inverter having an input coupled to an output of the differential amplifier.

30. A negative voltage level detector according to claim 25:

wherein the first voltage divider comprises:

a first resistor coupled between a reference voltage and the first input of the differential amplifier, and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal;

wherein the second voltage divider comprises:

a third resistor coupled between the reference voltage and the second input of the differential amplifier, and

a fourth resistor coupled between the second input of the differential amplifier and the negative voltage;

wherein the differential amplifier comprises:

a differential pair of input transistors coupled to the first and second input terminals,

a current source coupled to the differential pair of transistors, and

a load coupled to the differential pair of transistors; and

further comprising an inverter having an input coupled to an output of the differential amplifier.

31. A negative voltage level detector according to claim 25 wherein the differential amplifier comprises a current mirror load coupled to a power supply terminal.

32. A negative voltage level detector according to claim 25 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the negative voltage is a negative voltage source for negatively biasing a word line.

33. A negative voltage level detector for a semiconductor device comprising:

means for dividing a reference voltage, thereby generating a first divided signal;

means for dividing a negative voltage, thereby generating a second divided signal; and

means for amplifying the difference between the first and second divided signals.

34. A negative voltage level detector according to claim 33 wherein the means for dividing a reference voltage comprises:

a first resistor coupled between the reference voltage and a first input of the means for amplifying; and

a second resistor coupled between the first input of the means for amplifying and a power supply terminal.

35. A negative voltage level detector according to claim 33 wherein the means for dividing a negative voltage comprises:

a first resistor coupled between a reference voltage and a second input of the means for amplifying; and

a second resistor coupled between the second input of the means for amplifying and the negative voltage.

36. A negative voltage level detector according to claim 33 wherein the means for amplifying comprises a differential amplifier referenced to a power supply voltage.

37. A negative voltage level detector according to claim 33 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the negative voltage is a negative voltage for biasing a word line.

38. A negative voltage level detector for a semiconductor device comprising:

a differential amplifier having a first input and a second input;

a first voltage divider coupled to the first input of the differential amplifier and adapted to drive the first input of the differential amplifier responsive to a reference voltage, wherein the first voltage divider is adapted to maintain the first input of the differential amplifier at a positive voltage; and

a second voltage divider coupled to the second input of the differential amplifier and adapted to drive the second input of the differential amplifier responsive to a negative voltage, wherein the second voltage divider is adapted to maintain the second input of the differential amplifier at a positive voltage.

39. A negative voltage level detector according to claim 38 wherein the first voltage divider comprises:

a first resistor coupled between the reference voltage and the first input of the differential amplifier; and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal.

40. A negative voltage level detector according to claim 38 wherein the second voltage divider comprises:

a first resistor coupled between a reference voltage and the second input of the differential amplifier; and

a second resistor coupled between the second input of the differential amplifier and the negative voltage.

41. A method for detecting a negative voltage in a semiconductor device comprising:

dividing a reference voltage, thereby generating a first divided signal;

dividing the negative voltage, thereby generating a second divided signal; and

amplifying the difference between the first and second divided signals.

42. A method according to claim 41 wherein dividing the reference voltage comprises level shifting the reference voltage.

43. A method according to claim 41 wherein dividing the negative voltage comprises level shifting the negative voltage.

44. A method according to claim 41 wherein amplifying the difference between the first and second divided signals comprises referencing a differential amplifier to a power supply voltage.

45. A method according to claim 41 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the negative voltage is a negative voltage for biasing a word line.

46. A negative voltage regulator for a semiconductor device comprising:

a differential amplifier having a first input, a second input, and an output;

an output transistor coupled to the output of the differential amplifier and arranged to generate a second negative voltage from a first negative voltage;

a first voltage divider coupled to the first input of the differential amplifier; and

a second voltage divider coupled to the second input of the differential amplifier, and adapted to drive the second input of the differential amplifier responsive to the second negative voltage.

47. A negative voltage regulator according to claim 46 wherein the first voltage divider is adapted to drive the first input of the differential amplifier responsive to a reference voltage.

48. A negative voltage regulator according to claim 47 wherein the first voltage divider comprises:

a first resistor coupled between the reference voltage and the first input of the differential amplifier; and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal.

49. A negative voltage regulator according to claim 46 wherein the second voltage divider comprises:

a first resistor coupled between a reference voltage and the second input of the differential amplifier; and

a second resistor coupled between the second input of the differential amplifier and the second negative voltage.

50. A negative voltage regulator according to claim 46:

wherein the first voltage divider comprises:

a first resistor coupled between a reference voltage and the first input of the differential amplifier, and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal;

wherein the second voltage divider comprises:

a third resistor coupled between the reference voltage and the second input of the differential amplifier, and

a fourth resistor coupled between the second input of the differential amplifier and a the second negative voltage;

wherein the differential amplifier comprises:

a differential pair of input transistors coupled to the first and second input terminals,

a current source coupled to the differential pair of transistors, and

a load coupled to the differential pair of transistors; and

wherein the output transistor has a second terminal coupled to an output terminal of the differential amplifier.

51. A negative voltage regulator according to claim 46 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the second negative voltage is a negative voltage source for negatively biasing a word line.

52. A negative voltage regulator for a semiconductor device comprising:

means for generating a second negative voltage from a first negative voltage responsive to a drive signal;

means for dividing a reference voltage, thereby generating a first divided signal;

means for dividing the second negative voltage, thereby generating a second divided signal;

means for amplifying the difference between the first and second divided signals, thereby generating the drive signal.

53. A negative voltage regulator according to claim 52 wherein the means for dividing the reference voltage comprises:

a first resistor coupled between the reference voltage and a first input of the means for amplifying; and

a second resistor coupled between the first input of the means for amplifying and a power supply terminal.

54. A negative voltage regulator according to claim 52 wherein the means for dividing the second negative voltage comprises:

a first resistor coupled between a reference voltage and the second input of the means for amplifying; and

a second resistor coupled between the second input of the means for amplifying and the second negative voltage.

55. A negative voltage regulator according to claim 52 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the first negative voltage is a negative voltage for biasing a word line.

56. A negative voltage regulator for a semiconductor device comprising:

a differential amplifier having a first input, a second input, and an output;

an output transistor coupled to the output of the differential amplifier and arranged to generate a second negative voltage from a first negative voltage;

a first voltage divider coupled to the first input of the differential amplifier and adapted to drive the first input of the differential amplifier responsive to a reference voltage, wherein the first voltage divider is adapted to maintain the first input of the differential amplifier at a positive voltage; and

a second voltage divider coupled to the second input of the differential amplifier and adapted to drive the second input of the differential amplifier responsive to the second negative voltage, wherein the second voltage divider is adapted to maintain the second input of the differential amplifier at a positive voltage.

57. A negative voltage level detector according to claim 56 wherein the first voltage divider comprises:

a first resistor coupled between the reference voltage and the first input of the differential amplifier; and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal.

58. A negative voltage level detector according to claim 56 wherein the second voltage divider comprises:

a first resistor coupled between a reference voltage and the second input of the differential amplifier; and

a second resistor coupled between the second input of the differential amplifier and the second negative voltage.

59. A method for generating a first negative voltage in a semiconductor device comprising:

generating a second negative voltage;

dividing a reference voltage, thereby generating a first divided signal;

dividing the first negative voltage, thereby generating a second divided signal;

amplifying the difference between the first and second divided signals, thereby generating a drive signal; and

driving an output transistor coupled between the first negative voltage and the second negative voltage responsive to the drive signal.

60. A method according to claim 59 wherein dividing the reference voltage comprises level shifting the reference voltage.

61. A method according to claim 59 wherein dividing the first negative voltage comprises level shifting the first negative voltage.

62. A method according to claim 59 wherein amplifying the difference between the first and second divided signals comprises referencing a differential amplifier to the second negative voltage.

63. A method according to claim 59 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the first negative voltage is a negative voltage for biasing a word line.